CLAIMS

1. A method of fabricating a memory cell integrated in a semiconductor substrate comprising:

forming, on the semiconductor substrate, a MOS device having first and second conduction terminals;

forming a first protective layers over the MOS device;

forming and patterning one or more metallization layers over the MOS device;

forming a second protective layer over the one or more metallization layers;forming a capacitive element coupled in series with the MOS device, including defining a lower electrode of the capacitive element on the second protective layer, wherein the capacitive element is formed after all of the one or more metallization layers are formed and patterned without forming and patterning any additional metallization layer after the capacitive element is formed.

2. The method of claim 1 further comprising:

forming a plurality of contact vias through the first and second protective layers for establishing an electrical connection between the lower electrode of the capacitive element and at least one of the conduction terminals of the MOS device.

3. The method of claim 2 wherein forming a capacitive element comprises forming a ferroelectric capacitor having a ferroelectric material layer for a dielectric layer.

4. The method of claim 1, wherein the one or more metallization layers includes a first metallization layer formed on the first protective layer and a second metallization layer formed between the second protective layer and a third protective layer positioned between the first and second protective layers, the method further comprising forming a pad area from the second metallization layer and electrically connecting the pad area to an upper electrode of the capacitive element.

5. The method of claim 4 further comprising forming a flat on the second protective layer and electrically coupling the flat to the upper electrode of the capacitive element, and forming an electrical contact that extends through the second protective layer between the pad area to the flat.

6. The method of claim 1, wherein the one or more metallization layers includes a first metallization layer formed on the first protective layer and a second metallization layer formed between the second protective layer and a third protective layer positioned between the first and second protective layers, the method further comprising:

forming a pad area from the second metallization layer before forming the second protective layer; and

removing a portion of the second protective layer from the pad area after the capacitive element is formed, thereby exposing the pad area for an external connection.

7. The method of claim 1, wherein the one or more metallization layers includes a first metallization layer formed on the first protective layer and a second metallization layer formed between the second protective layer and a third protective layer positioned between the first and second protective layers, the method further comprising forming a third metallization layer on the second protective layer before forming the lower electrode on the second protective layer.

8. A method of making a memory cell integrated in a semiconductor substrate, the method comprising:

forming a MOS device;

forming a plurality of metallization layers including a first metallization layer, the plurality of metallization layers overlaying the MOS device;

covering the first metallization layer with a top insulating layer;

forming a capacitive element on the top insulating layer after forming the plurality of metallization layers, the capacitive element having a lower electrode covered with a layer of a dielectric material and capacitively coupled to an upper electrode;

forming a flat on the top insulating layer;

electrically connecting the flat to the upper electrode by a plate line; and

electrically connecting the flat to a pad of the first metallization layer such that the memory cell may be driven through the pad of the first metallization layer provided beneath the capacitive element.

9. The method of claim 8 wherein the flat and the lower electrode are formed by forming a conductive layer on the top insulating layer and defining the flat and the lower electrode from the conductive layer.

10. The method of claim 8, further comprising:

forming a bottom insulating layer on the substrate; and

forming a plurality of contact vias through the bottom and top insulating layers for establishing an electrical connection between the lower electrode of the capacitive element and a conduction terminal of the MOS device.

11. The method of claim 8 wherein electrically connecting the flat to the first metallization layer includes:

forming a pad area from the first metallization layer; and

forming a contact that extends through the top insulating layer and electrically connects the pad area to the flat.

12. The method of claim 11, wherein the pad area is formed before forming the top insulating layer, the method further comprising removing a portion of the top protective layer from the pad area after the capacitive element is formed, thereby exposing the pad area for an external connection.

13. The method of claim 1, further comprising forming a second metallization layer on the top protective layer and defining the second metallization layer into a first pad area before forming the lower electrode on the top insulating layer, and connecting the first pad area to a second pad area formed from the first metallization layer.

14. A method of forming a memory device integrated in a semiconductor substrate, the method comprising:

forming a matrix of memory cells each including a MOS device and a capacitive element, the matrix being formed by:

forming a plurality of metallization layers including a top metallization layer, the plurality of metallization layers being formed between the MOS devices and the capacitive elements of the memory cells;

covering the top metallization layer with a top insulating layer;

forming the capacitive elements on the top insulating layer after forming the plurality of metallization layers, each capacitive element having a lower electrode covered with a layer of a dielectric material and capacitively coupled to an upper electrode; and

forming a conductive flat on the top insulating layer and outside of the memory matrix; and

electrically connecting the flat to the upper electrodes of a plurality of the capacitive elements through a plate line that forms and connects the upper electrodes of the plurality of capacitive elements.

15. The method of claim 14, further comprising electrically connecting the flat to a pad of the first metallization layer such that the plurality of capacitive elements may be driven through the pad of the first metallization layer provided beneath the capacitive elements.

16. The method of claim 14 wherein the flat and the lower electrodes of the capacitive elements are formed by forming a conductive layer on the top insulating layer and defining the flat and the lower electrodes from the conductive layer.

17. The method of claim 14, wherein forming the matrix of memory cells includes:

forming a bottom insulating layer on the substrate; and

forming a plurality of contact vias through the bottom and top insulating layers for establishing an electrical connection between the lower electrodes of the capacitive elements and conduction terminals of the MOS devices.

18. The method of claim 14, further comprising:

forming a pad area from the first metallization layer; and

forming a contact that extends through the top insulating layer and electrically connects the pad area to the flat.

19. The method of claim 18, wherein the pad area is formed before forming the top insulating layer, the method further comprising removing a portion of the top protective layer from the pad area after the capacitive elements are formed, thereby exposing the pad area for an external connection.

20. The method of claim 14, further comprising forming a second metallization layer on the top protective layer and defining the second metallization layer into a first pad area before forming the lower electrodes on the top insulating layer, and connecting the first pad area to a second pad area formed from the first metallization layer.